What is claimed is:

1. A method of processing addresses, comprising:
receiving a full linear address of an instruction; and
reducing a size of the full linear address to obtain a reduced linear address.

2. The method of claim 1, further including hashing a subset of the full linear address to reduce the size of the full linear address.

3. The method of claim 2, wherein the full linear address includes one or more line offset bits and one or more set index bits, the method further including isolating the offset bits and the set index bits from the hashing.

4. The method of claim 2, further including hashing a thread signature with the subset of the full linear address.

5. The method of claim 1, further including retrieving a data block from a data array if the reduced linear address corresponds to a tag in a tag array, the tag array being associated with the data array.

6. The method of claim 5, wherein the data array is a prediction array of a branch predictor, the data block including a branch prediction address having a size that equals a size of the reduced linear address.

7. The method of claim 5, wherein the data array is a cache array of a cache, the data block including a stored linear address having a size that equals the size of the full linear address.

8. The method of claim 7, further including verifying that either the data block is consecutive with respect to a previous data block or the stored linear address corresponds to a calculated branch target address.

9. The method of claim 8, wherein the cache is an instruction cache, the method further including decoding the data block.

10. The method of claim 8, wherein the cache is a trace cache.

11. A method of retrieving data, comprising:

receiving a full linear address of an instruction;

reducing a size of the full linear address to obtain a reduced linear address, the reducing including hashing a subset of the full linear address;

isolating one or more cache line offset bits of the full linear address and one or more set index bits of the full linear address from the hashing; and

retrieving a data block from a data array if the reduced linear address corresponds to a tag in a tag array, the tag array being associated with the data array.

12. The method of claim 11, wherein the data array is a prediction array, the data block including a branch prediction address having a size that equals a size of the reduced linear address.

13. The method of claim 11, wherein the data array is a cache array, the data block including a stored linear address having a size that equals the size of the full linear address.

14. The method of claim 13, further including verifying that either the data block is consecutive with respect to a previous data block or the stored linear address corresponds to a calculated branch target address.

15. The method of claim 14, wherein the cache is an instruction cache, the method further including decoding the data block.

16. The method of claim 14, wherein the cache is a trace cache.

17. An address processing unit comprising:

a data structure having a data array and a tag array;

a reduction module to reduce a size of a full linear address of an instruction to obtain a reduced linear address; and

a retrieval module to retrieve a data block from the data array if the reduced linear address corresponds to a tag in the tag array.

18. The address processing unit of claim 17, wherein the reduction module is to hash a subset of the full linear address to reduce the size of the full linear address.

19. The address processing unit of claim 18, wherein the full linear address is to include one or more line offset bits and one or more set index bits, the reduction module to isolate the offset bits and the set index bits from the hashing.

20. The address processing unit of claim 17, wherein the data array is a prediction array of a branch predictor, the data block to include a branch prediction address having a size that equals a size of the reduced linear address.

21. The address processing unit of claim 17, wherein the data array is a cache array of a cache, the data block to include a stored linear address having a size that equals a size of the full linear address.

22. The address processing unit of claim 21, further including an allocation module to verify that either the data block is consecutive with respect to a previous data block or the stored linear address corresponds to a calculated branch target address.

23. The address processing unit of claim 22, wherein the cache is an instruction cache, the architecture further including a decoder to decode the data block.

24. The address processing unit of claim 22, wherein the cache is a trace cache.

25. A computer system comprising:

a random access memory;

a bus coupled to the memory; and

a processor coupled to the bus, the processor to receive an instruction from the memory and including an address processing unit having a data structure, a reduction module and a retrieval module, the data structure having a data array and a tag array, the reduction module to reduce a size of a full linear address of the instruction to obtain a reduced linear address, the retrieval module to retrieve a data block from the data array if the reduced linear address corresponds to a tag in the tag array.

26. The computer system of claim 25, wherein the reduction module is to hash a subset of the full linear address to reduce the size of the full linear address.

27. The computer system of claim 26, wherein the full linear address is to include one or more line offset bits and one or more set index bits, the reduction module to isolate the offset bits and the set index bits from the hashing.